

File: g:\VSS_Projects\work\sjensen\DPA\hdl_project\src\Synchronizer.v

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1  *****
2  ****//
3  // file : c:\projects\nmc\DPA\hdl\DPAinterface\src\Synchronizer.v
4  // created Tue Oct 30 07:13:30 2001
5  // by ITF2V generator version 1.0
6  *****
7  ****//
8
9  //{{ Section below this comment is automatically maintained
10 // and may be overwritten
11 //{module {Synchronizer}}
12 module Synchronizer ( DAVE ,clk ,reset_DAVE ,reset ,set_DAVE ,
13 spi_clk );
14 input clk ;
15 wire clk ;
16 input reset_DAVE ;
17 wire reset_DAVE ;
18 input reset ;
19 wire reset ;
20 input set_DAVE ;
21 wire set_DAVE ;
22 input spi_clk ;
23 wire spi_clk ;
24
25 output DAVE ;
26 wire DAVE ;
27
28 //}} End of automatically maintained section
29
30 // -- Enter your statements here -- //
31 reg spi_side;
32 reg clk_side;
33
34 assign DAVE = spi_side ^ clk_side;
35
36 always @ (posedge reset or posedge clk)
37 begin
38     if (reset) clk_side <= 1'b0;
39     else if (reset_DAVE) clk_side <= spi_side;
40     else clk_side <= clk_side;
41 end
42
43 always @ (posedge reset or posedge spi_clk)
44 begin
45     if (reset) spi_side <= 1'b0;
46     else if (set_DAVE) spi_side <= !clk_side;
47     else spi_side <= spi_side;
48 end
49
50 endmodule
51
```